Amendments to the Claims

1. (Currently Amended) A system for testing an integrated circuit (IC) device having a power supply pin and at least one input pin, comprising:

a power supply configured to supply a maximum voltage;

a current measuring device for measuring current between the power supply and the IC device; and

an overvoltage source operative to apply an overvoltage pulse, wherein the overvoltage pulse is applied to a test pin of the at least one input pin and the maximum supply voltage is applied to each other input pin of the at least one input pin, the current measuring device detecting whether a latch up condition exists by detecting an increase in current between the power supply and the IC device based on application of the overvoltage pulse.

2. (Original) The system of claim 1, further comprising a switching system configured for sequentially connecting each input to be tested to the overvoltage source while each other input pin is connected to the power supply.

3. (Original) The system of claim 1, the current measuring device configured to detect a latch up condition by detecting a current increase of about at least three milliamps.

4. (Original) The system of claim 1, the current measuring device further comprises:

a first current measuring device for measuring current between the power supply and the power supply pin; and

a second current measuring device for measuring current between the power supply and the each other input pin of the at least one input pin.

5. (Original) The system of claim 4, the current measuring device detecting a latch up condition by detecting an increase in current in at least one of the first current measuring device and the second current measuring device upon application of the overvoltage pulse.

6. (Original) The system of claim 4, the overvoltage source configured to supply an overvoltage pulse with at least one of about a four nanosecond ramp time, about an eleven nanosecond pulse width, and about a four nanosecond drop time.

7. (Currently Amended) The system of claim 1, the IC device comprises a Complementary Metal-Oxide Semiconductor (CMOS) voltage tolerant electrostatic discharge device with a maximum power supply voltage of about 3.3 volts, the trigger overvoltage source configured to supply an overvoltage pulse greater than about 3.3 volts and less than about 11 volts.

8. (Currently Amended) A system for testing an integrated circuit (IC) device having a power supply pin and at least one input pin, comprising:

a power supply configured to supply a maximum voltage;

a current measuring device for measuring current between the power supply and the IC device;

an overvoltage source operative to apply an overvoltage pulse, wherein the overvoltage pulse is applied to a test input pin of the at least one input pin and the maximum supply voltage is applied to each other input pin of the at least one input pin, the current measuring device detecting whether a latch up condition exists by detecting an increase in current between the power supply and the IC device based on application of the overvoltage pulse; and

a switching system configured for sequentially connecting each input pin to be tested to the overvoltage source while each other input pin is connected to the power supply.

9. (Original) The system of claim 8, the current measuring device further comprises:

a first current measuring device for measuring current between the power supply and the power supply pin; and

a second current measuring device for measuring current between the power supply and the each other input pin of the at least one input pin.

10. (Original) The system of claim 9, the current measuring device detecting a latch up condition by detecting an increase in current in at least one of the first current measuring device and the second current measuring device upon application of the overvoltage pulse.

11. (Currently Amended) A system for testing a device, the device comprising a power supply input and a plurality of inputs, the system comprising:

means for supplying a maximum supply voltage;

means for measuring current from the means for supplying a maximum supply voltage to the device;

means for generating an overvoltage pulse;

means for selecting a test input by coupling a test input of the plurality of inputs to the means for generating an overvoltage [source] pulse and coupling each other input of the plurality of inputs to the means for supplying a maximum supply voltage; and

means for determining a latch up condition[ing] by detecting an increase in current from the [power supply] means for supplying a maximum supply voltage upon application of the overvoltage pulse to the test input.

12. (Currently Amended) The system of claim 11, the means for measuring current further comprising:

means for measuring current between the [power supply] means for supplying a maximum supply voltage and the power supply input; and

means for measuring current between the [power supply] means for supplying a maximum supply voltage and the each other input of the plurality of inputs.

13. (Currently Amended) The system of claim 12, the means for determining [an increase in current from the power supply] a latch up condition by detecting the increase from at least one of the means for measuring current between the [power supply] means for supplying a maximum supply voltage and the power supply input, and the means for measuring current between the power supply and the each other input of the plurality of inputs.

14. (Original) The system of claim 11, the means for selecting a test input comprising sequentially selecting each of the other plurality of inputs for overvoltage testing.

15. (Original) A method for testing an integrated circuit (IC) device with a power supply input, a plurality of inputs and a plurality of outputs, the method comprising:

applying a maximum supply voltage to the power supply input;

applying maximum supply voltage to the plurality of inputs;

selecting a test pin by decoupling an input of the plurality of inputs from the maximum supply voltage and applying an overvoltage pulse to the test pin; and

detecting whether a latch up condition exists by detecting whether current to the IC device increased upon applying the overvoltage pulse.

16. (Original) The method of claim 15, the detecting a latch up condition further comprising:

performing a first current measurement to the device before applying the overvoltage pulse;

performing a second current measurement to the device after applying the overvoltage pulse; and

comparing the first current measurement and the second current measurement to determine if a current increase to the IC device has occurred.

17. (Original) The method of claim 15, the detecting whether current to the IC device increased upon applying the overvoltage pulse comprising detecting whether current increased from at least one of the current to the power supply input and the current to the plurality of inputs.

18. (Original) The method of claim 15, further comprising sequentially selecting a new test input from the plurality of inputs for each of the plurality of inputs by coupling the test input to the maximum supply voltage, decoupling the new test input from the maximum supply voltage and applying an overvoltage pulse to the new test pin.

19. (Original) The method of claim 15, the detecting whether a latch up condition exists comprises determining whether the current increased by about at least three milliamps.

20. (Original) The method of claim 15, the overvoltage pulse having at least one of about a four nanosecond maximum rise time, about an eleven nanosecond maximum pulse width, and about a four nanosecond maximum drop time.